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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,951	04/02/2004	Greg A. Blodgett	M4065.0285/P285-C	8919

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EXAMINER	
NGUYEN, TAN	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,951	BLODGETT, GREG A.	
	Examiner	Art Unit	
	Tan T. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *56-73* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *58* is/are allowed.

6)☒ Claim(s) *56,57 and 59-72* is/are rejected.

7)☒ Claim(s) *58, 73* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/02/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The Preliminary amendment submitted by Applicant on April 2, 2004 has been received and entered.

2. The Information Disclosure Statement submitted by Applicant on April 2, 2004 has been received and fully considered.

3. Claims 1-55 have been canceled.

New claims 56-73 have been added.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 56-57, 59, 61-62, 64-67, 69-72 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. (U.S. Patent No. 6,330,190).

Wang et al. disclosed in Figure 2A a flash memory cell in a program mode wherein a programming voltage is applied between a respective drain [26] and a gate [21] by connecting a voltage no greater than +9 volts, preferably +6.5 volts to the control gate [21], while the drain [26] is connected to a positive supply of +5.0 volts, or less, preferably +4 volts (column 6, lines 20-24). As the memory cell is in program mode, hot electrons are trapped in the floating gate [20] which charges the floating gate negatively. The negative charge changes the threshold voltage of the transistor. In this manner the memory cell is programmed (column 5, lines 45-48). As the threshold voltage of the memory cell changes from one value to another value, the state or identity of the memory cell is also changes from one state or identity to another identity.

Wang et al. further disclosed in a read operation, a positive potential, typically Vcc or +5 volts is applied to the control gate [21] and a +1 volt is applied to the bit lie which is coupled to the drain [26]. The presence, or absence, of electrons on floating gate [29] makes the transistor harder, or easier, to turn on, and this condition is detected by the bit line connected to the drain [26]. If the transistor turns on, the bit line is discharged to ground. The state of the bit line is then determined as a "one" or zero" (column 6, lines 38-47).

Regarding claims 59, 65-67, Wang et al. disclosed in the program operation, a preferred voltage of +6.5 v is applied to the control gate via the word line, and a preferred voltage of +4.5 v is applied to the drain via the bit line. The word line would be considered as the claimed first signal line, the bit line would be considered as the claimed second signal line.

Regarding claim 61, Wang et al. did not discuss the specific normal threshold voltage of the transistor in the memory cell, however, it is inherent that the normal threshold voltage value of a transistor is approximately 0.7 V, and the memory cell, before being programmed to a specific state, inherently has no negative charge trapped in the floating gate which results the threshold voltage of the memory cell has normal value.

Regarding claim 62, as the memory being program by the programming method of Wang et al. negative charge trapped in the floating gate which inherently increases the threshold voltage of the memory cell.

Regarding claim 64, the "one" or "zero" state in program operation disclosed by Wang et al. in column 6, lines 42-47 would be understood as the claimed "on" or "off" state.

Regarding claims 69-70, Wang et al. did not disclose what voltage is applied to the source of the memory cell, which inherently teaches the source of the memory is connected to ground or left floating.

Regarding claim 71, Wang et al. disclosed in the read operation that the flow of current in the memory cell is sensed to indicate the state of the memory cell.

Regarding claim 72, the voltages applied to the drain (1 V) and to the control gate (5 V) are greater than the normal threshold voltage value of transistor (.7 V).

6. Claims 57 and 69-72 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimoji (U.S. Patent No. 5,463,579).

Shimoji disclosed in Figure 4c a reading operation for a memory in which a potential [Vc] of 5V is applied to a control gate [8], and a potential [Vd] of 1V is applied to the drain of the cell. Current does not flow between the source region [2] and the drain region [3] if the cell is in the erased state, in which the floating gate [6] holds electrons injected so that the threshold voltage is relatively high. Alternatively, current floes between the source region [2] and the drain region [3] if the cell is in written state in which electron have been withdrawn from floating gate [6] so that the threshold voltage is relatively low. Therefore, by determining whether or not current flows, the storage state "1" or "0" can be read (column 6, line 56 to column 7, line 1).

Regarding claims 69-70, Shimoji disclosed the source region [2] of the memory cell is being grounded in read operation (column 6, line 59).

Regarding claim 71, Shimoji disclosed by determining whether or not current flows, the storage state, "1" or "0" can be read (column 6, line 67 to column 7, line 1).

Regarding claim 72, the voltage applied to the control gate [8] (5V) and the voltage applied to the drain region [3] (1V) are greater than the normal threshold voltage value of the transistor (0.7V).

7. Claims 57, 69-72 are rejected under 35 U.S.C. 102(b) as being anticipated by Thomas (U.S. Patent No. 5,506,431).

Thomas disclosed a read operation for a memory cell in Figure 3 in which a voltage typically in the range of 0.5 to 2.5 V is applied to the drain [4], and a second voltage typically from 2 to 5 V is applied to the word line formed on the control gate [10] and sensing the current in the cell. If the cell is in written condition, typically with negative charge accumulated on the floating gate [8], the threshold voltage (Vt) of the device will be high and the current flow will be small. If it is an erased cell with zero charge in the floating gate, the voltage coupled down to the floating gate [8] from the control gate will turn the cell on and a cell current will flow in the bit line. This information is sensed and used to indicate the state of the cell (column 5, lines 35-48).

Regarding claims 69-70 Thomas did not disclose what voltage is applied to the source of the memory cell, which inherently teaches the source of the memory is connected to ground or left floating.

Regarding claim 71, Thomas disclosed in the read operation that the flow of current in the memory cell is sensed to indicate the state of the memory cell.

Regarding claim 72, the voltages applied to the drain (0.5-2.5 V) and to the control gate (2-5 V) are greater than the normal threshold voltage value of transistor (.7 V).

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 60 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al..

See description of Wang et al. in paragraph 5, supra. Wang did not disclose how long the programming voltage is applied as in claim 60, nor the specific value of the second value.

It appears that how long the programming voltage is applied or what the specific of the second value of the threshold voltage of the memory cell are matters of design choice.

It would have been obvious to a person of ordinary skill of the art at the time the invention was made to modify the programming operation disclosed by Wang et al. by selecting appropriate time interval and appropriate value for the threshold voltage of the memory cell.

The rationale is as follows: A person of ordinary skill in the art would have been motivated to select an appropriate time interval for the programming operation to optimize the programming operation, and selecting a desired value for the threshold voltage of the memory to distinguish the different states of the memory cells.

10. Claims 68 ad 73 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Claim 58 is allowed.

The following is an examiner's statement of reasons for allowance: The prior art failed to show or suggest the step of changing an output of the address decoder in response to an output signal of a transistor after being programmed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

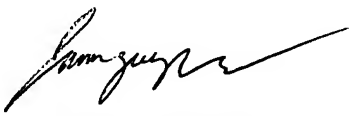
Banks is cited to show memory device having different conductivity states of the cell are provided as information storage states for the cells. Kaya is cited to show it is possible to set the threshold voltage of an EEPROM to any value by varying the amount of charge residing on the floating gate. Kodama is cited to show in programming, as the

injected electrons trapped in floating gate, the threshold voltage shifts in the positive direction (column 3, lines 30-34).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms, can be reached at (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tan T. Nguyen
Primary Examiner
Art Unit 2818
July 30, 2004